	Type	L #	Hits	Search Text	DBs
1	BRS	L1	19875	(etching or etched or etch or etches or remove or removal or removing or removed or removes) same (exposed or expose or exposure) same (conductive or conductor or floating)	USPAT
2	BRS	L2	504	1 same (cmp)	USPAT
3	BRS	L3	98	2 same (trenches or trench)	USPAT
4	BRS	L4	1570	(etching or etched or etch or etches or remove or removal or removing or removed or removes) same (exposed or expose or exposure) same (floating)	USPAT
5	BRS	L5	31	4 same (cmp)	USPAT
6	BRS	L6	29	(etching or etched or etch or etches or remove or removal or removing or removed or removes) same ((stopping or stopped) near5 floating)	USPAT
7	IS&R	L7	691	(438/424).CCLS.	USPAT
8	BRS	L8	691	7 not (6 or 5)	USPAT
9	BRS	L9	30	8 and floating	USPAT
10	IS&R	L10	644	(438/257).CCLS.	USPAT
11	BRS	L11	630	10 not (5 or 6 or 9)	USPAT
12	IS&R	L12	385	(438/258).CCLS.	USPAT
13	BRS	L13	310	12 not 10	USPAT
14	BRS	L14	57	13 and (trench near3 (isolation or isolating or insulation))	USPAT
15	BRS	L15	30321	(nonvolatile or non-volatile) near3 memory	USPAT
16	BRS	L16	441	15 and (trench near3 (isolation or isolating or Insulation))	USPAT
17	BRS	L17	352	16 not (14 or 13 or 12 or 10)	USPAT

	Type	L #	Hits	Search Text	DBs
1	BRS	L2	3299	(etching or etch or etches or etched or removing or remove or removal or removed or removes) near10 ((trench or trenches) near3 (Isolation or isolating or insulating or insulator or hdp or oxide))	USPAT
2	BRS	L3	916	floating near5 (stopping or stop or stopped)	USPAT
3	BRS	L4	0	2 near15 3	USPAT
4	BRS	L5	0	2 same 3	USPAT
5	BRS	L6	8	2 and 3	USPAT
6	BRS	L7	0	humped adj2 transistor	USPAT

DOCUMENT-IDENTIFIER: US 6034393 A
TITLE: Nonvolatile semiconductor memory device using trench isolation and manufacturing method thereof

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BSPR:
Referring to FIGS. 19 and 20, when thick oxide film 106 deposited in trench 105
or floating gate 103 is to be removed by the CMP method so as to fill trench
105 with thick oxide film 106, floating gate 103 is made thinner to be the thin
floating gate 103 as shown in FIG. 20, since the etching rate of floating gate
103 formed of polycrystalline silicon under the CMP method is faster than the
etch rate of thick oxide film 106 under the CMP method. At this time, floating
gate 103 is not only physically etched by the CMP method but it has its surface
exposed to an alkali solution used in the CMP. Therefore, the upper surface of
floating gate 103 and inner portion of floating gate 103 near the upper surface
are physically and chemically damaged.

BSPR:
When thick oxide film 106 is to be filled in trench 105 not by the CMP method
but by dry etch back method, the upper surface of floating gate 103 is exposed
to etching plasma in the dry etch back method. Therefore, the upper

surface of
floating gate 103 and inner portion of floating gate 103 near the upper surface
suffer from plasma damage of dry etching.